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LETTER TO THE EDITOR

Evidence for excess vacancy defects in the Pd–Si system: positron annihilation, x-ray diffraction and Auger electron spectroscopy study

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Abstract
The transformation of Pd/Si to Pd_2Si/Si is investigated using depth-resolved positron annihilation, x-ray diffraction and Auger electron spectroscopy studies. The observed defect-sensitive positron S-parameter value of 1.022–1.054 indicates the existence of divacancies across the silicide/silicon interface and Si substrate region. Our experimental observation of vacancy defects is consistent with the model proposed for excess vacancy generation across the interface consequent to Si diffusion.

The metal silicide system [1, 2] has been a topic of intense basic and technological interest. At a fundamental level, the formation of metal silicide involves the diffusion of either one or both the species across the interface for chemical reaction at elevated temperatures. In the case of the Pd–Si system, there is substantial evidence supporting Si to be the faster diffusing species [1–3]. On a microscopic scale, the formation of a silicide layer can lead to the production of point defects, namely interstitials and vacancies, in the silicon region as proposed by Wen *et al* [4]. The silicide layer so formed can further influence the generation and removal of point defects across the interface, which is also an important issue. Italyantsev and Kuznetsov [5] proposed a model wherein there is excess vacancy generation at the silicide/silicon interface consequent to enhanced silicon diffusion. Experimental results pointing towards the displacement of Si and its interstitial diffusion due to silicidation in Cu/Re/Si system [6] and the role of Cu interstitials in Cu_3Si formation [7] have been reported. In this letter, we provide for the first time clear evidence for the production of excess vacancy defects across the silicide–silicon interface as well as in the Si substrate, using defect-sensitive positron annihilation with corroborative x-ray diffraction (XRD) and Auger electron spectroscopy (AES) studies in the Pd/Si system.

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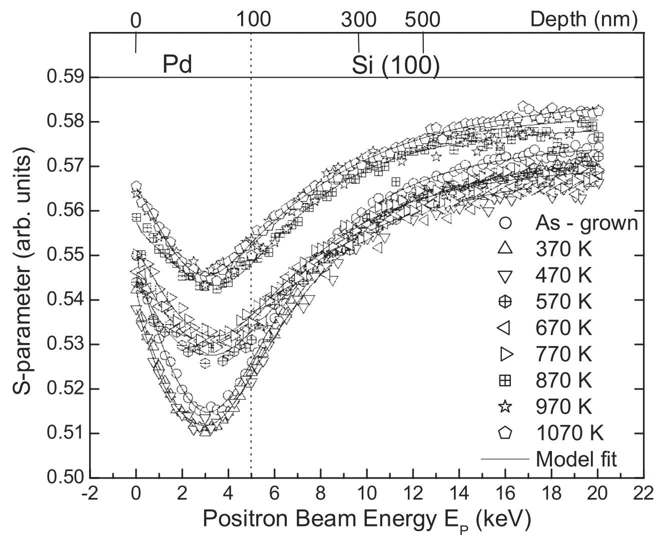

Figure 1. S-parameter versus positron beam energy E_p curves for various annealing temperatures. The curve drawn through the data points is the result of model fitting using the VEPFIT program. The vertical dotted line indicates the location of the initial Pd/Si interface.

An Si(100) wafer of thickness 500 μm was coated with a Pd layer at room temperature using an electron beam evaporation system in a vacuum of 10^{-7} Torr. Prior to deposition, the substrate was cleaned for removal of the SiO_2 layer by a standard HF acid etching procedure. The thickness of the evaporated Pd layer was monitored using an *in situ* quartz crystal monitor and found to be about 65 nm, while independent Rutherford back scattering (RBS) measurements deduced the thickness to be 100 $\pm$ 10 nm. This wafer was cut into small samples and annealed at various temperatures between 370 and 1070 K in steps of 100 K in a vacuum of 2×10^{-6} Torr. Depth-resolved Doppler broadening of 511 keV annihilation γ-ray measurements [8, 9] were carried out on as-grown and annealed samples. The measurements were made at room temperature using a compact magnetically guided positron beam system [10]. By varying the positron energy E_p (0–20 keV), the positron beam can be implanted at various depths of the sample starting from the near-surface region up to a depth of $\sim$1.5 μm. Positrons, implanted at selected depths, get thermalized and annihilate with the medium giving rise to a 511 keV γ-ray spectrum, which is Doppler broadened. From the measured spectrum, a defect-sensitive lineshape S-parameter [8, 9], namely, the ratio of counts in the central portion (511 $\pm$ 1 keV) of the curve to the total photopeak counts (511 $\pm$ 10 keV), was deduced at each E_p. It has been established that the presence of open-volume defects at the site of positron annihilation increases the S-parameter value [8, 9]. The raw experimental S versus E_p curves were fitted by solving the positron diffusion equation, using the VEPFIT program [11]. Conventional XRD studies were also carried out on the same samples to obtain independent evidence for silicide phase formation. AES measurements were carried out in a UHV analysis chamber, using a cylindrical mirror analyser (CMA) based spectrometer with 0.4% energy resolution. Prior to the AES study, the samples were sputtered *in situ* using 500 eV Ar ions.

The variation of the S-parameter as a function of positron beam energy for various annealing temperatures is shown in figure 1. The depth scale probed by the positron beam is indicated on the top axis. The following features are noticed:

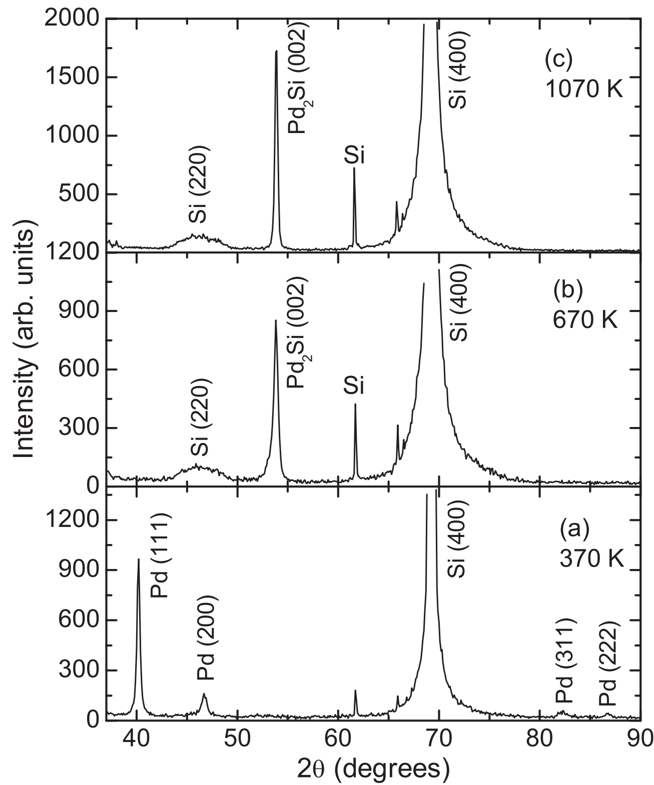

Figure 2. Selected XRD spectra of Pd–Si samples annealed at 370, 670 and 1070 K. Reference peaks due to pure Pd and Si are also shown.

(i) the initial reduction with a minimum at 3 keV and subsequent increase in S-parameter up to 5 keV corresponds to the Pd-layer;
(ii) the interface is located at 5 keV; and
(iii) the further increase beyond 5 keV and the saturation behaviour of the S-parameter beyond 12 keV corresponds to that of the silicon substrate.

The S-parameter versus E_p variation is consistent with the annihilation characteristics arising as the positron beam traverses from high S-parameter region of the near-surface layer $\rightarrow$ low S-parameter region of the metallic Pd layer $\rightarrow$ high S-parameter region of the semiconducting Si layer. Due to diffusional broadening of the positron implantation profile, there is no abrupt change in S-parameter across the interface at 5 keV. Three broad temperature regimes are noticed in S versus E_p variation, as the annealing temperature is increased.

(a) From the as-grown state to 470 K, the S-parameter corresponding to the Pd layer decreases slightly, indicating the annealing of structural defects in the as-grown layer. In this temperature range, the XRD pattern (shown in figure 2(a)) indicates the characteristic lines due to the Pd and Si substrate.
(b) Beyond 570 K, the S-parameter corresponding to the Pd layer increases and the observed S-parameter variation is constant up to 770 K. Over this temperature interval, XRD measurements, as shown in figure 2(b), revealed the existence of Pd_2Si and Si peaks, while Pd peaks were absent. This indicates the complete conversion of Pd/Si to Pd_2Si/Si.

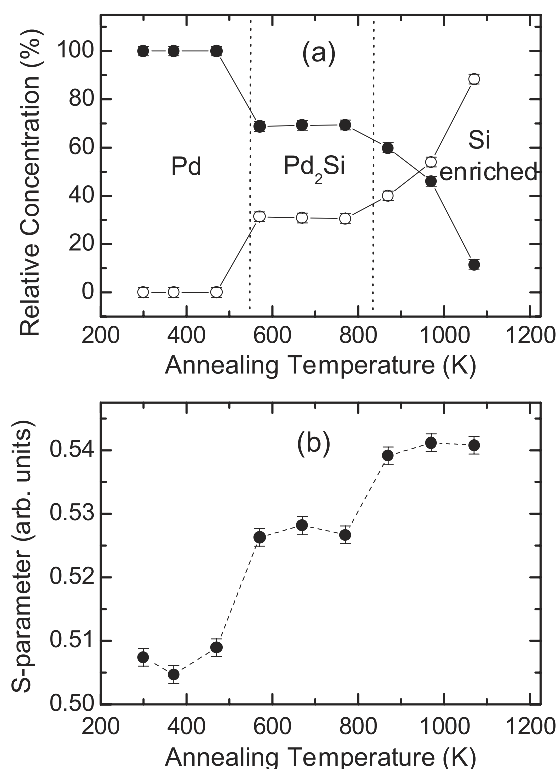

Figure 3. (a) AES results of the relative surface concentration of Pd (solid circles) and Si (open circles) as a function of annealing temperature. The three temperature regimes corresponding to Pd, Pd_2Si and Si-enriched Pd_2Si are separated by vertical dotted lines. (b) Positron annihilation data in terms of the VEPFIT-resolved *S*-parameter of the first layer, showing characteristic changes similar to AES trends. The dashed line through the data points is a guide to the eye.

The present results of the formation of the Pd_2Si phase beyond 570 K are in accordance with earlier results reported using XRD, AES and TEM [1, 12].

(c) Beyond 870 K, the *S*-parameter between the near-surface to 5 keV further increases and its variation is almost constant up to 1070 K. A large increase in the *S*-parameter of the interfacial region is also noticeable. Even the substrate *S*-parameter values (beyond 12 keV) are larger. On the other hand, in the same temperature range, XRD (figure 2(c)) has indicated only Pd_2Si and Si lines, with no further phase formation.

Based on this, the observed *S*-parameter changes in the silicide region can be attributed to enhanced Si diffusion from the interfacial region to the silicide region, resulting in the production of vacancy defects at interfacial and substrate regions. These aspects are discussed below.

We provide AES evidence for the presence of excess Si concentration in the silicide layer, which indicates enhanced Si diffusion from the interface to surface regions at higher temperatures. The relative surface concentrations of Pd (MNN transition—330 eV) and Si (LMM transition—92 eV) as a function of annealing temperature are shown in figure 3(a). Consistent with the XRD and positron annihilation results, only the Pd signature is seen up to 470 K. Beyond 570 K, we find Pd_2Si formation i.e., Pd—67% and Si—33%, which corresponds to the stoichiometric composition of Pd_2Si. Above 870 K, the Si concentration is found to

increase steeply beyond the stoichiometric value. In view of the same silicide phase being observed by XRD in this temperature range, we attribute the increase in Si concentration beyond 870 K to be due to Si diffusion into Pd_2Si. Our results of enhanced Si diffusion into the silicide from the Si region are in agreement with marker experiments on Pd/Si [13]. AES studies on Cu/Re/Si [6] have also shown that silicidation aids rapid diffusion of Si from the substrate region into the silicide region. Due to this enhanced Si diffusion from the substrate region, there should be vacancy production preferentially at the silicide/silicon interface.

We now present model fitting of positron annihilation data by numerical solution of the positron diffusion equation using the VEPFIT program [11]. In this analysis, apart from the surface state, positron annihilation at different layers, namely the Pd layer, silicide layer, interfacial defect layer and Si substrate layer, is taken into account for fitting the experimental data shown in figure 1. For the data up to 470 K, only two layers, i.e., the Pd layer and the Si layer, were sufficient. For higher temperatures, another intermediate layer, having relatively higher S-parameter than the first layer, had to be invoked to fit the data. The existence of this interfacial layer, consequent to silicide formation, points to the presence of vacancy defects at the interface between the silicide and Si layers. The variation of the S-parameter of the first layer is shown in figure 3(b). Consistent with the AES results, we find that the S-parameter of the first layer shows up distinct changes attributable to the existence of the Pd layer, silicide formation and Si enrichment of the silicide due to enhanced Si diffusion. For temperatures beyond 870 K, the S-parameter exhibits rather a flat behaviour, while AES (figure 3(a)) is able to sense the changes in Si concentration of the top surface, due to its higher elemental sensitivity.

So as to present evidence for the existence of vacancy defects at the interface and substrate layers, the variation of the normalized S-parameter of these layers, as a function of annealing temperature, is shown in figure 4. The normalization is done with respect to the corresponding values at 570 K. The interfacial S-parameter gradually increases as the annealing temperature is increased and reaches a value of 1.054 ± 0.0015 by 1070 K. The S-parameter of the Si-substrate layer is typically around 1.00 up to 770 K, and beyond 870 K it increases and reaches a value of 1.0227 ± 0.0015. The S-parameter values, well above the normalized value of 1.00, are a clear indication for the existence of vacancy defects. The S-parameter value ranges from 1.054 in the interfacial region to 1.0227 in the substrate region around 1070 K. We now attempt to estimate the size of the vacancy defects by comparing the present S-parameter values with that of *ab initio* calculations for the S-parameter in crystalline Si [14]. The calculations indicate a value of 1.018 for V_1, 1.045 for V_2, 1.053 for V_3 and 1.067 for V_4. Experimental S-parameters in the range of 1.015–1.04 have been reported for divacancies in the literature [9, 15]. Since monovacancies in Si are highly mobile, and at room temperature only divacancies are found to be stable, we would like to assign the present S-parameter values in the range of 1.022–1.054 to the presence of divacancies. It may be seen that S-parameter values are larger at the interfacial region than at the substrate region. We would like to ascribe the higher interfacial S-parameter to the larger concentration of divacancy defects. In view of their higher mobility, divacancies, produced at the interface, diffuse into the Si substrate region beyond 870 K, thereby increasing the S-parameter value of the substrate region to 1.022. In fact, Italyantsev and Kuznetsov [5] model calculations also indicate an excess vacancy production at the interface and a concentration gradient for vacancy defects between the interface and Si substrate regions. The model predicts that vacancy defects can diffuse as far as 500 nm from the interface, at annealing temperature beyond 870 K. The present positron annihilation results are consistent with the model predictions.

Depth-resolved positron annihilation measurements along with corroborative XRD and AES studies are reported on Pd/Si samples annealed at various temperatures. Silicide phase

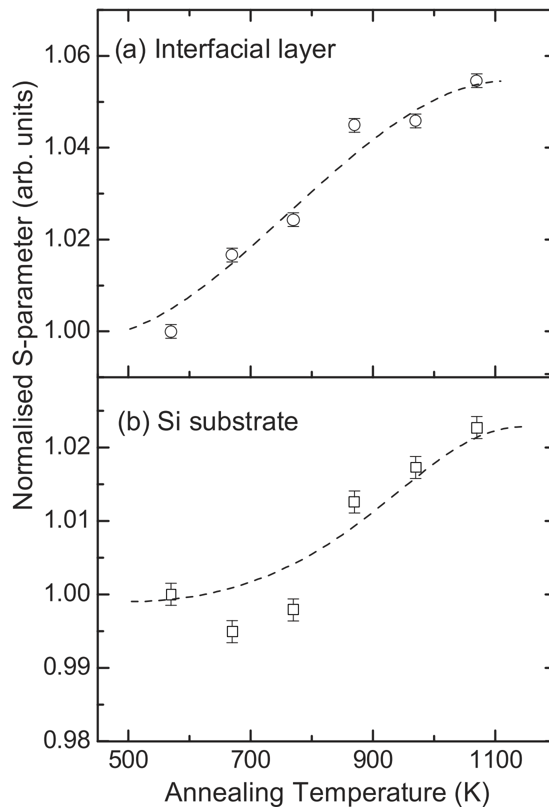

Figure 4. Results of positron diffusional analysis of the experimental data. Normalized *S*-parameter of (a) the interfacial defected layer and (b) the Si substrate layer as a function of annealing temperature. The dashed line through the data points is a guide to the eye.

formation is evident from XRD, AES and positron annihilation. The evidence for enhanced Si diffusion is obtained from AES, while the existence of vacancy defects is deduced from positron annihilation studies. Large *S*-parameter values observed at the silicide/silicon interface clearly point to the existence of divacancies, whose concentration increases at higher temperatures. Divacancies are found to diffuse from the interface into Si substrate regions. The present experimental results support the prevailing models of silicide formation and excess vacancy generation.

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